

CSEE 4280: Lab 2:

Design, Simulating & Implementing a 4-Bit ALU

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Contributions: Please list contributions (in estimated percentages) of each member in the following categories.

• Pre-lab design and analysis:

Habilou - 50% Kingsley - 50%

• In-lab module and testbench design

Habilou - 50% Kingsley - 50%

• In-lab testbench simulation and analysis

Habilou - 50% Kingsley - 50%

• In-lab FPGA synthesis and analysis

Habilou - 50% Kingsley - 50%

• Lab report writing

Habilou - 50% Kingsley - 50%

# **ABSTRACT**

1. **INTRODUCTION**
2. **IMPLEMENTATION DETAILS**
3. **EXPERIMENTAL RESULTS**
4. **SIGNIFICANCE**
5. **CONCLUSION**